REMARKS

Claim 12 is amend to correct a typographical error by changing "a bus" to "the bus".

Claim Rejections - 35 USC § 112

Claims 18 and 19 are rejected under 35 USC 112, second paragraph, as lacking antecedent basis for "the memory bus." Claims 18 and 19 are amended to provide proper antecedent basis.

Claim Rejections - 35 USC § 102

Claims 1-4, 11-23 are rejected under 35 USC 102(b) as being anticipated by Ludwig, et al. Applicants traverse this rejection.

Claim 1 is amended to recite that the buffer is not stacked with the memory devices. Ludwig teaches a buffer that is part of the stack of memory devices so that it fits into the same footprint as a single memory device. Therefore, claim 1 is not anticipated by Ludwig.

Claim 11 is also amended to recite that the buffer is not stacked with the first and second memory devices. Therefore, claim 11 is not anticipated by Ludwig.

Claim 12 is amended to recite that the module is fabricated on a circuit board. Ludwig does not disclose a module fabricated on a circuit board. Ludwig only discloses a module made from stacked chip components (col. 2, line 6).

Claim 14 (which has been rewritten in independent form) recites that the memory module is adapted to redrive a signal to another memory module. Claim 15 is amended to depend from claim 14. Claim 15 recites that the memory module is adapted to redrive a plurality of signals to another memory module. Claim 16 (also rewritten in independent form) recites that the buffer is adapted to redrive a signal to another memory module. Ludwig does not disclose any method or apparatus for redriving a signal or signals to other memory modules. Therefore, claims 14-16 are not anticipated by Ludwig.

Claim 17 is amended to recite that the memory devices are not stacked on the buffer. Claim 18 is amended to recite that the stacks of memory devices are not stacked on the buffers. Again, Ludwig only teaches a buffer that is part of the stack of memory devices. Therefore, claims 17 and 18 are not anticipated by Ludwig.

Claim 19 recites a second buffer coupled between the second stack of memory devices and the first buffer. Ludwig does not disclose a second buffer arranged in this manner.

Claim 23 recites that the bus is fabricated on a circuit board and the buffer is mounted on the circuit board. Ludwig only discloses a module made from stacked chip components (col. 2, line 6). Therefore, claim 23 is not anticipated by Ludwig.

New Claims

New claims 24-32 are added. These claims recite various arrangements having multiple stacks of memory devices per buffer and are, therefore, allowable over the prior art.

Applicant requests reconsideration in view of the foregoing amendments and remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears than an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Amended once) A memory system comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices, wherein the buffer is not stacked with the first and second memory devices.

11. (Amended once) A memory module comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus, wherein the buffer is not stacked with the first and second memory devices.

12. (Amended once) A memory module [according to claim 11 further comprising] comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus;

wherein the module is fabricated on a circuit board and further comprises a connector attached to the [module] circuit board and adapted to couple the module to [a] the bus.

14. (Amended once) A memory module [according to claim 11] comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus;

wherein the memory module is adapted to receive a signal from the bus and to redrive the signal to another memory module.

15. (Amended once) A memory module according to claim [11] 14 wherein the memory module is adapted to receive a plurality of signals from the bus and to redrive the plurality of signals to another memory module.

16. (Amended once) A memory module [according to claim 11] comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus;

wherein the buffer is adapted to receive a signal from the bus and to redrive the signal to another memory module.

17. (Amended once) A memory system comprising:

a bus;

a stack of memory devices; and

a buffer coupled between the stack of memory devices and the memory bus, wherein the stack of memory devices is not stacked on the buffer.

18. (Amended twice) A memory system comprising:

a bus;

a stack of memory devices;

a buffer coupled between the stack of memory devices and the [memory] bus;

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the bus;

wherein the stacks of memory devices are not stacked on the buffers.

19. (Amended twice) A memory system comprising:

a bus;

a stack of memory devices;

a first buffer coupled between the stack of memory devices and the [memory] bus;

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the first buffer.

Claims 24-32 have been added as new claims.